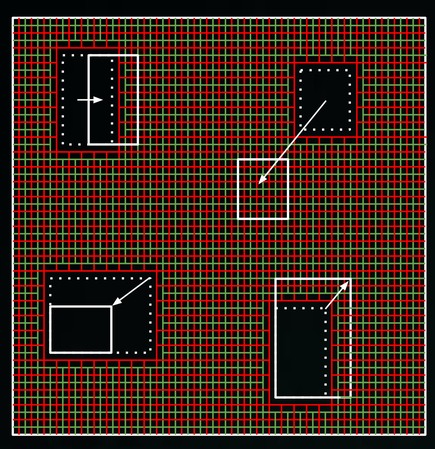
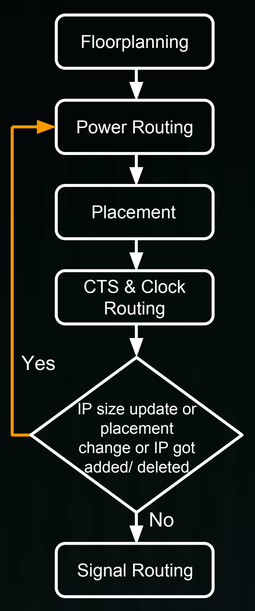
Incremental Power Routing at Different Phases of Physical Design Flow

Jagadeeshwar Surigi

Motivation

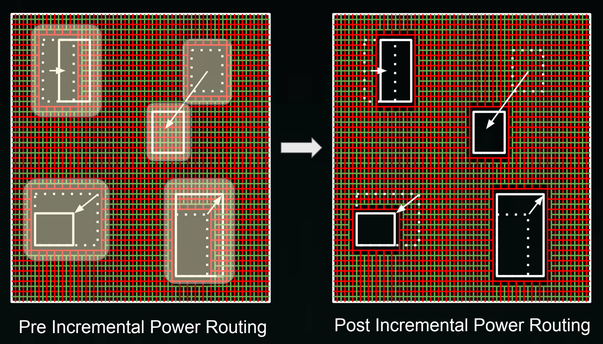
- Time to market pushes all domains, chip/IP/block/tool/methodology etc., to work in parallel. In today's ever evolving complex ASIC chips, changes during the design cycle are inevitable. Any floorplan change causes severe disruption in the physical design flow which could lead to project delay. A quick automated method was needed to accomplish incremental power routing to absorb such changes.





Previous location of IP/block
Current location of IP/block
Iterative process

Automated Incremental Power Routing

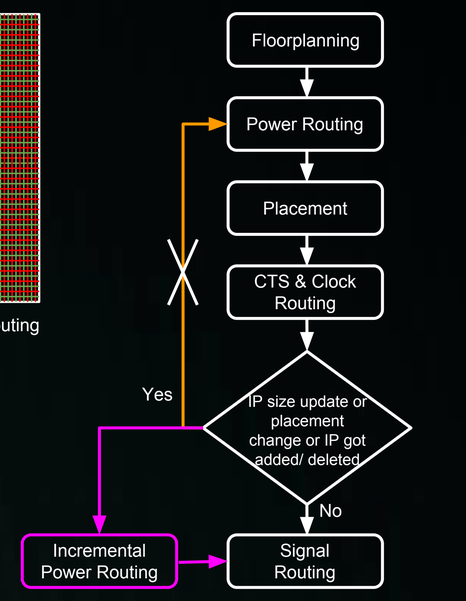


Pre Incremental Power Routing

Post Incremental Power Routing

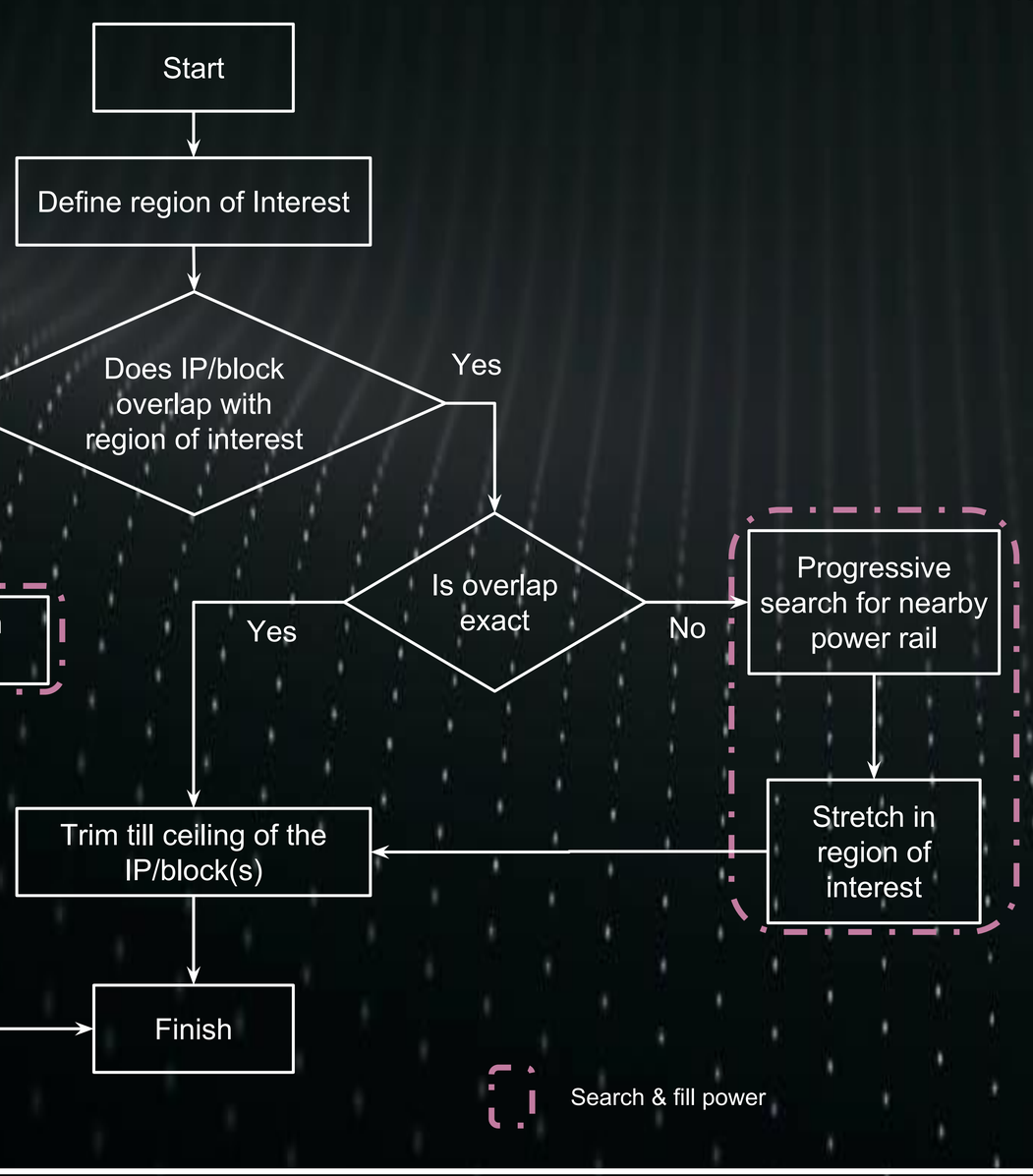
Area of Interest
Previous location of IP/block
Current location of IP/block

- Automated method, works only in a restricted region which is impacted due to floorplan changes, for ensuring the power continuity
- Method ensures minimal disturbance in the existing infrastructure of power rails/wires/placement etc. of the design
- Can mitigate floorplan change which includes size/shape/placement change of IP/block(s), even addition and/or deletion of IP/block(s), by filling in or cutting out power rails
- Saves significant time by working in small area

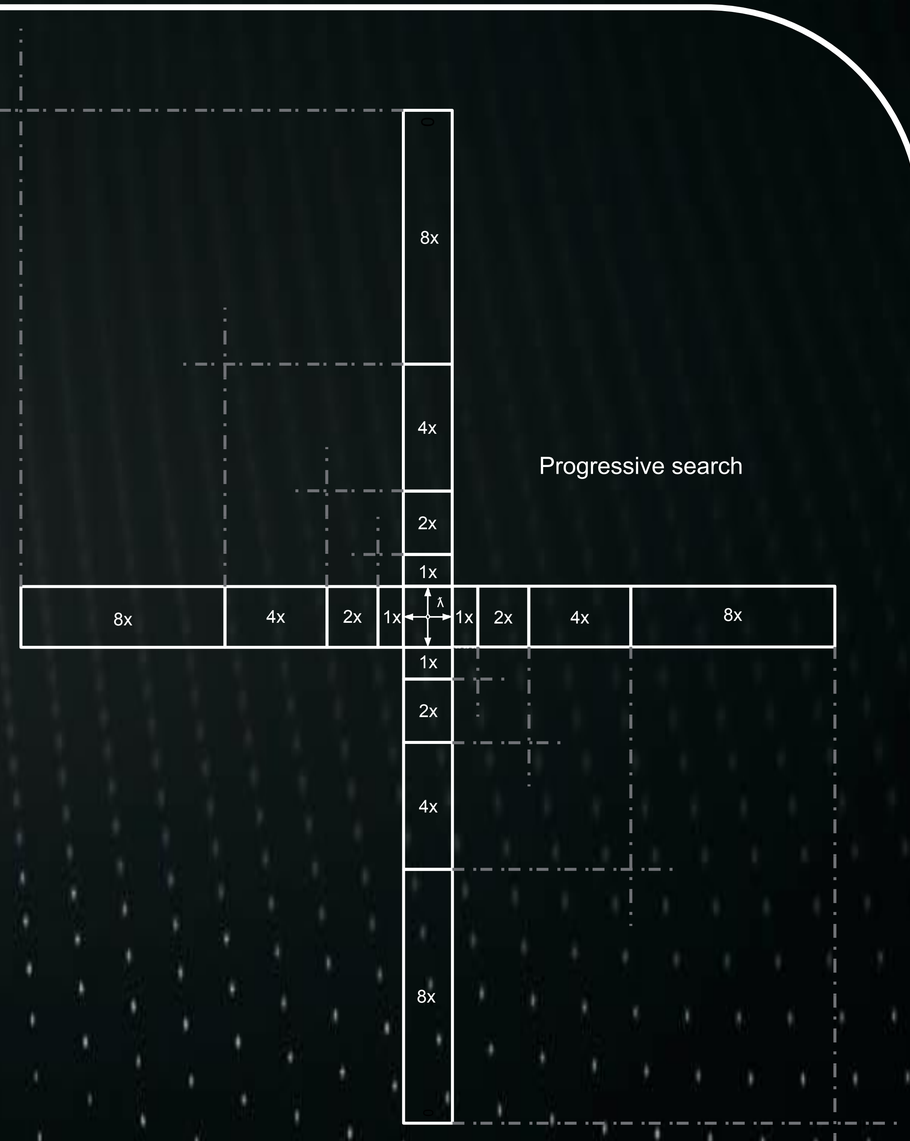


Proposed procedure
Iterative process

Algorithm



Search & fill power



$y = 2^{(n-1)}x$ equation for progressive search
x step size
λ initial step

Evidence

Void is formed due to block movement (or deletion), incremental power routing closes with required power rails

Power routes over the block are trimmed by incremental power routing

❖ Incremental power routing procedure reduces runtime as the region where re-power routing is performed is reduced

Summary

- Automated method enables designer to accommodate changes at various stages of design cycle
- Procedure compliant with DRC
- Significant TAT reduction achieved, from hours to minutes
- Technology independent
- Supports all scenarios of floorplan changes with respect to IP/block(s)

Planned future work

- Enabling ringed blocks
- Support for multi power domain designs

averasemi